

TILT.400 – REVISIONS

1

SCH REV	PCB REV	DATE	BY	DESCRIPTION	PCB REV	DATE	BY
0.0		02 DEC 31	wsk	START			
0.01		03 JAN 23	wsk	Sheet 2: Added notes and Jumper table; Sheet 3: Modified M1 pin assignments (3-5); Added JP17,RP3;			
1.00	1.00	03 JAN 27	wsk	Sheet 7: Changed Reference Designators P4 & P6 to J/P1A & J/P1B;			
2.00	2.00	03 MAY 12	wsk	Sheet 3: Added P4; Sheet 5: Changed C19 to B size package; Changed U5 to SO8 package; Added P4; Sheet 7: Swapped J/P1A & J/P1B; Sheet 8: Changed C14 to 0603 package;			
2.10	2.10	03 JUL 16	wsk	PCB: Corrected wiring error at serial 0 / serial 4;			
2.11	2.10	03 SEP 26	wsk	Sheet 6: Replaced missing intersheet connector;			
2.12	2.10	03 OCT 14	wsk	Sheet 2: Corrected Note 5;			
2.12	2.11	03 NOV 18	wsk	PCB: Added rubber foot mounting locators to bottom silkscreen;			
2.13	2.11	03 DEC 10	wsk	Sheet 5: Changed C19 to 16V;			
2.14	2.11	04 JUL 26	wsk	Sheet 2: Added Note 6; Sheet 3: Added Embedlet Connector annotation; Sheet 4: Corrected JSimm / SimmStick Connector definition; Added note; Sheet 5: Corrected U7 component type; Sheet 6: Renamed this sheet; Marked C20, C21, & U15 as NOT NORMALLY STUFFED; Corrected intersheet reference; Added Device Code table;			

3

3

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TABLE OF CONTENTS

SHEET	TITLE
1	REVISIONS
2	NOTES
3	Simm72 INTERFACE
4	JSimm INTERFACE
5	NETWORK I/O
6	1-WIRE I/O
7	SERIAL I/O
8	POWER & RESET

TO DO:


SPI, i2C, 1-wire, Vraw, +5, GND possibly a net board JSimm.proto.net
i2c xcver package change

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Title		TILT.400 REVISIONS
Size	Number	Rev
B		2.13
Date		Mon Jul 26, 2004
Drawn by		wsk
Filename	TILT_400_214.sch	Sheet 1 of 8

4

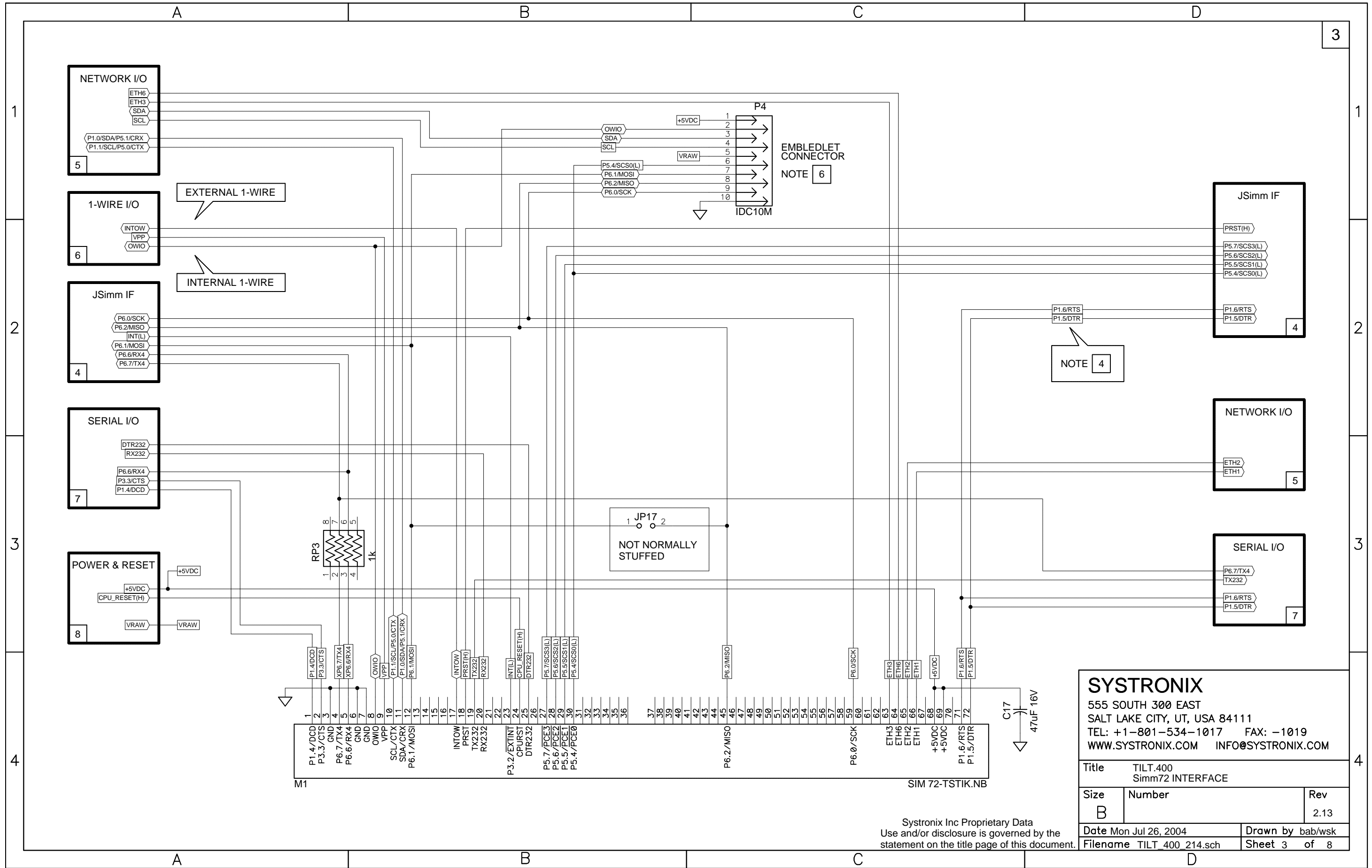
4

JUMPERS				2																										
JUMPER	CONDITION	DESCRIPTION	SHEET	NOTES																										
1	JP1	SHORTED	ROUTES TStik SERIAL 4 TO JSimm SERIAL B. SEE JP6	4	1 JSimm pin definition is compliant with the SimmStick (TM) specification.																									
	4	OPEN	ROUTES TStik SERIAL 4 TO JSimm SERIAL A. SEE JP6		2 SimmStick (TM) specification for pin 4 PWR, is 7.5 - 18Vdc.																									
	JP2	SHORTED	CONNECTS I2C BUFFER/REPEATER (U5) TO TStik	5	3 JP8 / JP16 SELECTS THE 1-WIRE PROGRAMMING VOLTAGE (VPP) SUPPLY SOURCE. JP8 IS NOT STUFFED AT MANUFACTURING.																									
		OPEN	CONNECTS CAN TRANSCEIVER (U7) TO TStik		IF A PROGRAMMING VOLTAGE (VPP) IS REQUIRED, OPEN JP16 AND INSTALL A 3-PIN JUMPER AT JP8. FOR NORMAL OPERATION INSTALL A SHORTING BLOCK AT JP8 PINS 1-2 TO CONNECT +5VDC TO THE TStik.72.NB DS2480 VPP PIN.																									
	JP3	SHORTED	TERMINATES CAN BUS	7	WHEN THE PROGRAMMING VOLTAGE IS REQUIRED INSTALL A SHORTING BLOCK AT JP8 PINS 2-3. OPEN JUMPER JP12 TO PROTECT U9 FROM VPP. BEFORE APPLYING VPP ENSURE THAT THE DEVICE IN S1 AND ANY DEVICES CONNECTED TO P3, P5 AND M2 (JSimm) ARE RATED FOR VPP. VPP MUST BE APPLIED TO THE SYSTEM BEFORE VCC.																									
	JP4	SHORTED	CONNECTS VRAW TO CAN BUS. CAN BUS CAN SOURCE RECIEVE POWER THROUGH THIS JUMPER.		4 SIGNAL CLASH MAY OCCUR IF U10 IS ENABLED WHEN ANOTHER DEVICE IS INSTALLED IN THE JSimm SOCKET (M2). CHECK THE JUMPERS JP1 AND JP6.																									
2	JP5	SHORTED	ASSERTION OF SERIAL 0 DTR CAUSES TStik RESET WHEN INSTALLED	8	5 RJ-12 (P3) IS STANDARD DALLAS 1-WIRE ASSIGNMENT. DALLAS NUMBERS THE PINS DIFFERENTLY FROM RJ-12 MANUFACTURERS. REGARDLESS OF NUMBERING CONVENTION THE PHYSICAL LOCATION OF SIGNAL IS THE SAME ON DALLAS & SYSTRONIX BOARDS.																									
	JP6	SHORTED	DISABLES (TRI-STATES) SERIAL 4 RS-232 TRANSCEIVER SEE JP1		 <table border="1" data-bbox="2253 836 2486 1038"> <thead> <tr> <th colspan="3">1-WIRE PIN NUMBERS</th> </tr> <tr> <th>SYSTRONIX</th> <th></th> <th>DALLAS</th> </tr> </thead> <tbody> <tr> <td>6</td> <td>VRAW</td> <td>1</td> </tr> <tr> <td>5</td> <td>N/C</td> <td>2</td> </tr> <tr> <td>4</td> <td>GND</td> <td>3</td> </tr> <tr> <td>3</td> <td>1-WIRE</td> <td>4</td> </tr> <tr> <td>2</td> <td>GND</td> <td>5</td> </tr> <tr> <td>1</td> <td>VCC</td> <td>6</td> </tr> </tbody> </table>				1-WIRE PIN NUMBERS			SYSTRONIX		DALLAS	6	VRAW	1	5	N/C	2	4	GND	3	3	1-WIRE	4	2	GND	5	1
1-WIRE PIN NUMBERS																														
SYSTRONIX		DALLAS																												
6	VRAW	1																												
5	N/C	2																												
4	GND	3																												
3	1-WIRE	4																												
2	GND	5																												
1	VCC	6																												
	JP7	NC PASTE*	FOR MANUFACUTURING USE ONLY	8																										
	JP8	1-2	CONNECTS +5VDC TO VPP. REQUIRED IF JP16 IS OPEN.	6	6 http://sourceforge.net/projects/embedlets																									
		2-3	CONNECTS +12VDC TO VPP. JP16 MUST BE OPEN.																											
	JP9	1-2	NOT NORMALLY STUFFED: CONNECTS EXTERNAL 1-WIRE NET TO iBUTTON SOCKET S1	5																										
		2-3	CONNECTS INTERNAL 1-WIRE NET TO iBUTTON SOCKET S1. JP14 SHOULD BE OPEN.																											
3	JP10	-	CONTROLS CAN TRANCEIVER MODE. SEE NOTE ON SHEET 5.	5																										
	JP11	NC PASTE*	FOR MANUFACUTURING USE ONLY	6																										
JP12	SHORTED	CONNECTS EXTERNAL 1-WIRE TO U9. OPEN THIS JUMPER WHEN JP8 PINS 2-3 ARE CLOSED.	6																											
	JP13	-	FOR MANUFACUTURING USE ONLY																											
	JP14	NC PASTE*	PARALLELS JP9 1-2. CONNECTS iBUTTON SOCKET S1 TO EXTERNAL 1-WIRE NET.																											
	JP15	NC PASTE*	PARALLELS JP10 1-2. CONTROLS CAN TRANSCEIVER MODE. SEE NOTE ON SHEET 5.	5																										
4	JP16	NC PASTE*	PARALLELS JP8 1-2. CONNECTS +5VDC TO VPP. MUST BE OPEN WHEN JP8 2-3 ARE CLOSED.	6																										
	JP17	SHORTED	REQUIRED FOR DALLAS TINI-390 OR IMSYS SNAP. CONNECTS CE0 TO RCE0. SPI NOT AVAILABLE.	3																										

* NC PASTE JUMPERS ARE SHORTED DURING MANUFACTURING. THESE JUMPERS MAY BE OPENED IN THE FIELD.

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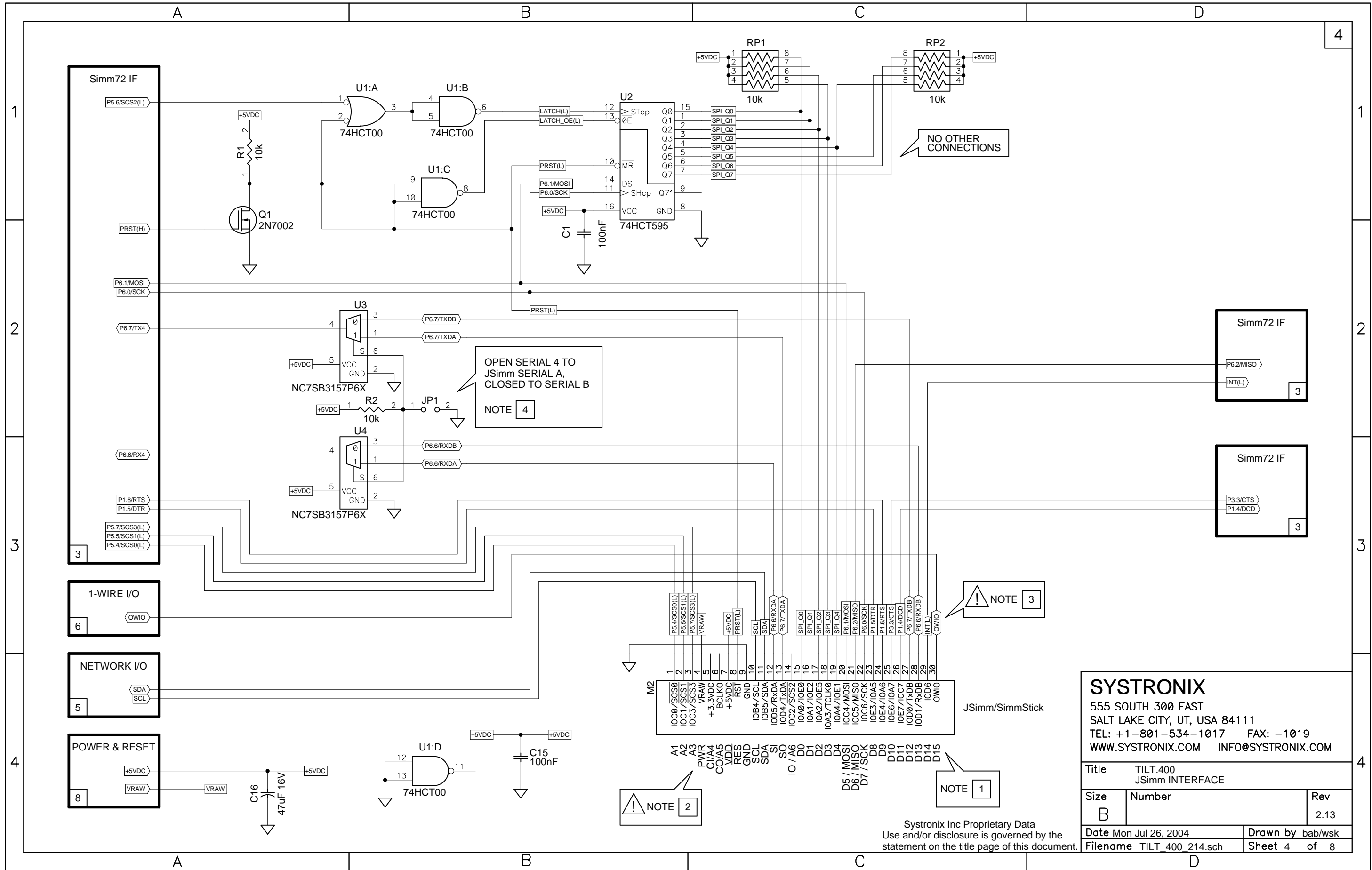
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Size	Number	Rev
B		2.13
Date	Mon Jul 26, 2004	Drawn by wsk
Filename	TILT_400_214.sch	Sheet 2 of 8



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Date	Mon Jul 26, 2004	Drawn by bab/wsk
Filename	TILT_400_214.sch	Sheet 3 of 8

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NO OTHER CONNECTIONS

OPEN SERIAL 4 TO JSimm SERIAL A, CLOSED TO SERIAL B
NOTE 4

NOTE 3

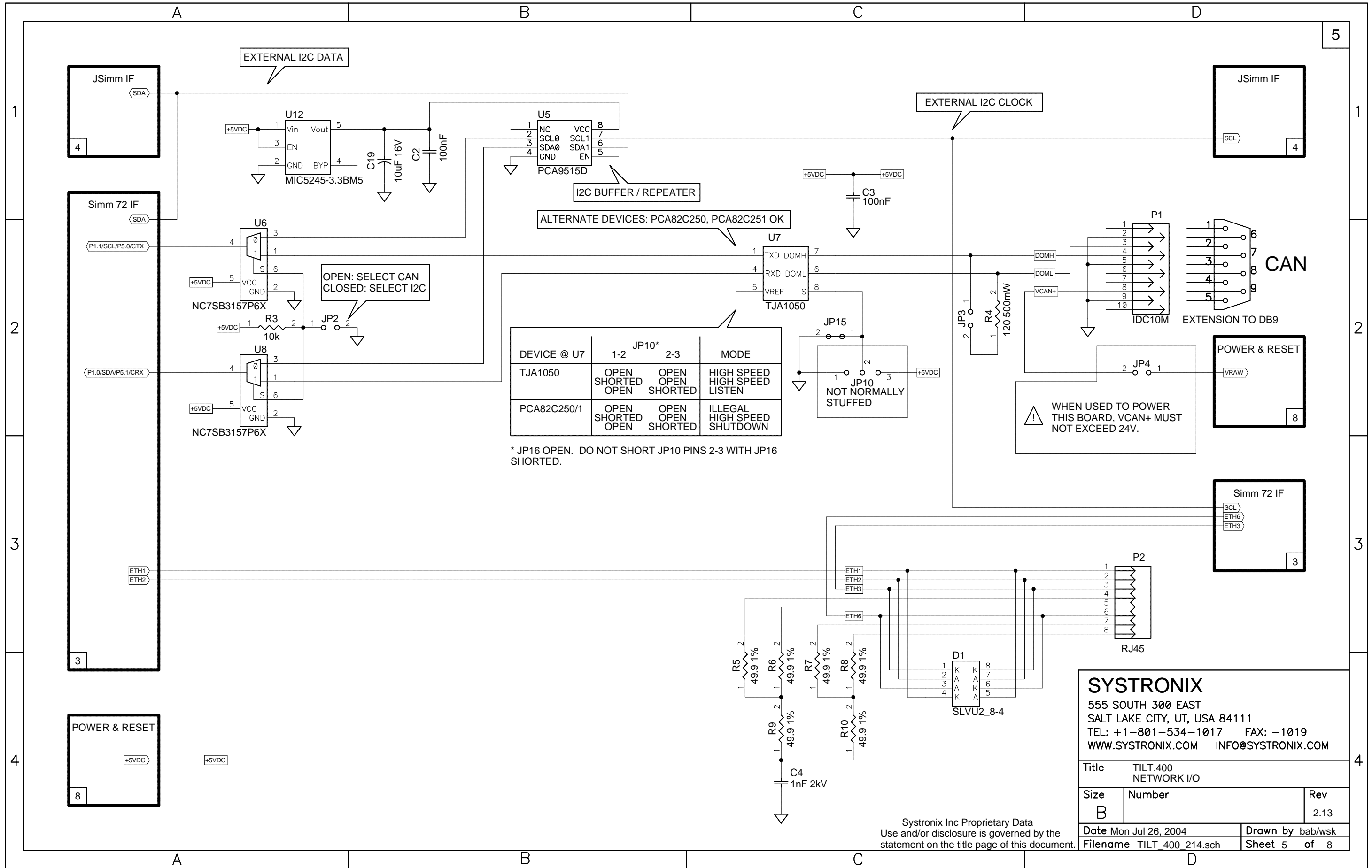
NOTE 2

NOTE 1

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Size B	Number	
Date Mon Jul 26, 2004	Drawn by bab/wsk	Sheet 4 of 8
Filename TILT_400_214.sch		

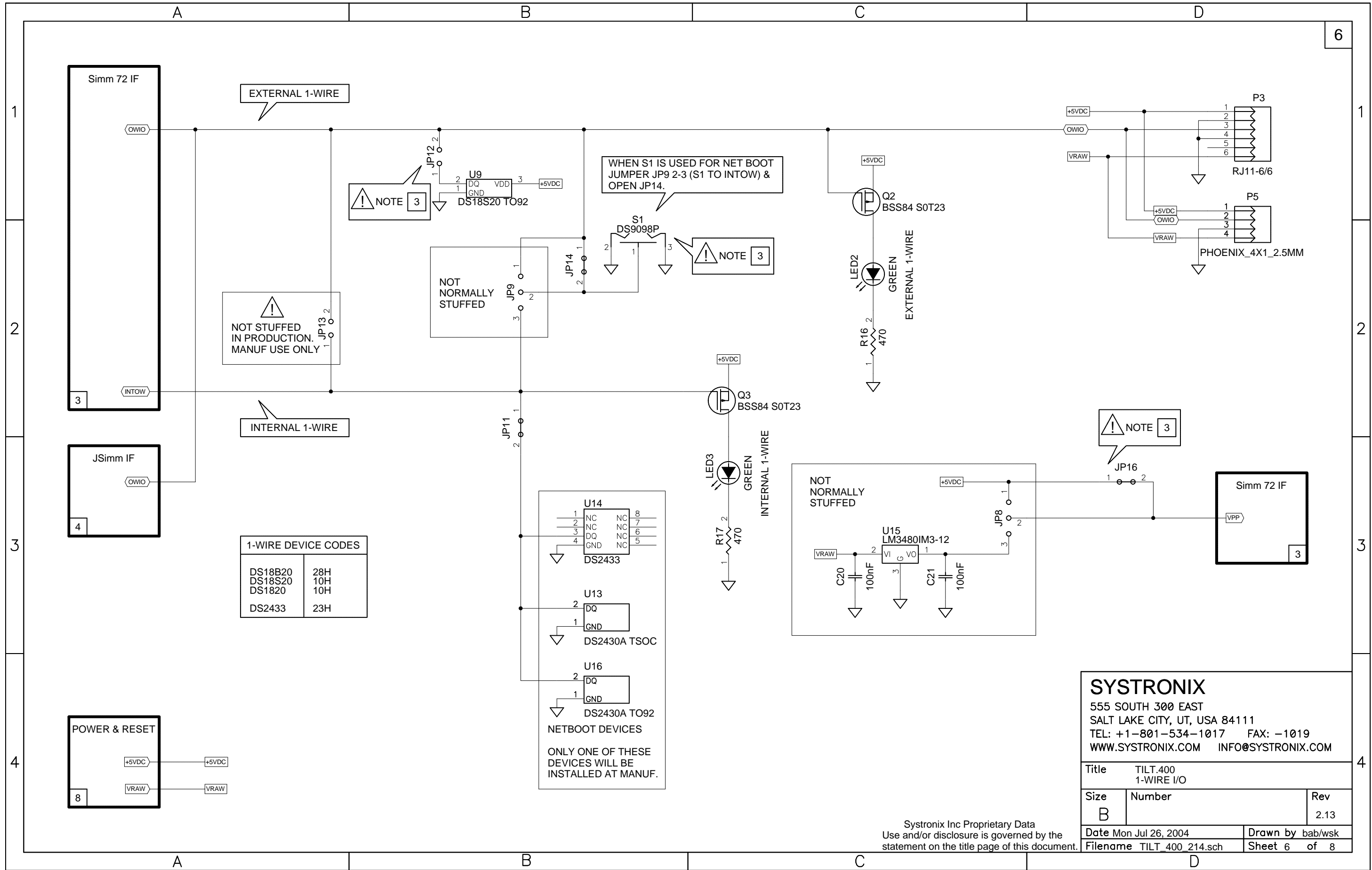


DEVICE @ U7	1-2 JP10*	2-3	MODE
TJA1050	OPEN SHORTED OPEN	OPEN OPEN SHORTED	HIGH SPEED HIGH SPEED LISTEN
PCA82C250/1	OPEN SHORTED OPEN	OPEN OPEN SHORTED	ILLEGAL HIGH SPEED SHUTDOWN

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Size	Number	Rev
B		2.13
Date	Mon Jul 26, 2004	Drawn by bab/wsk
Filename	TILT_400_214.sch	Sheet 5 of 8

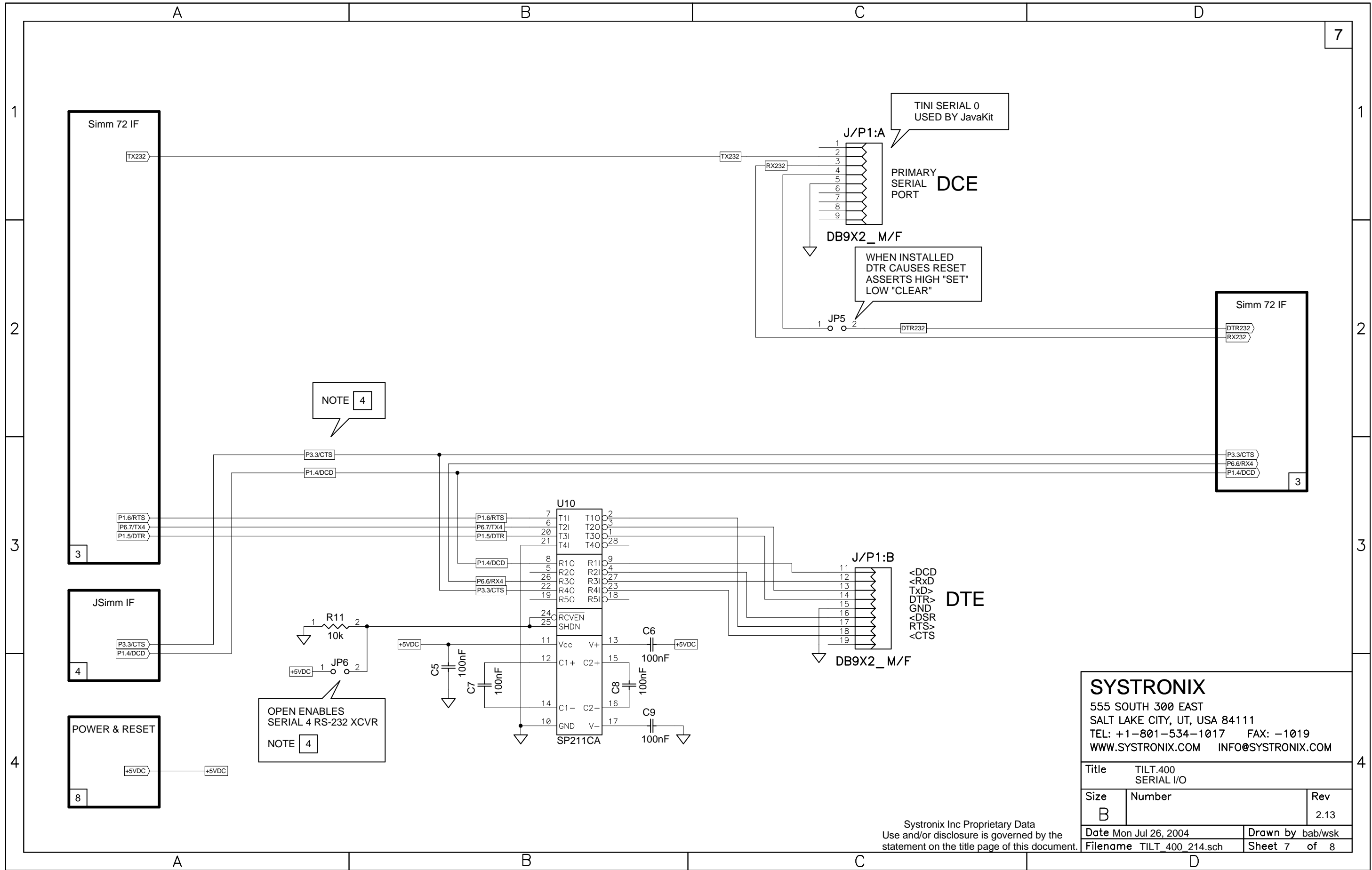
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Filename TILT_400_214.sch	Sheet 6 of 8	

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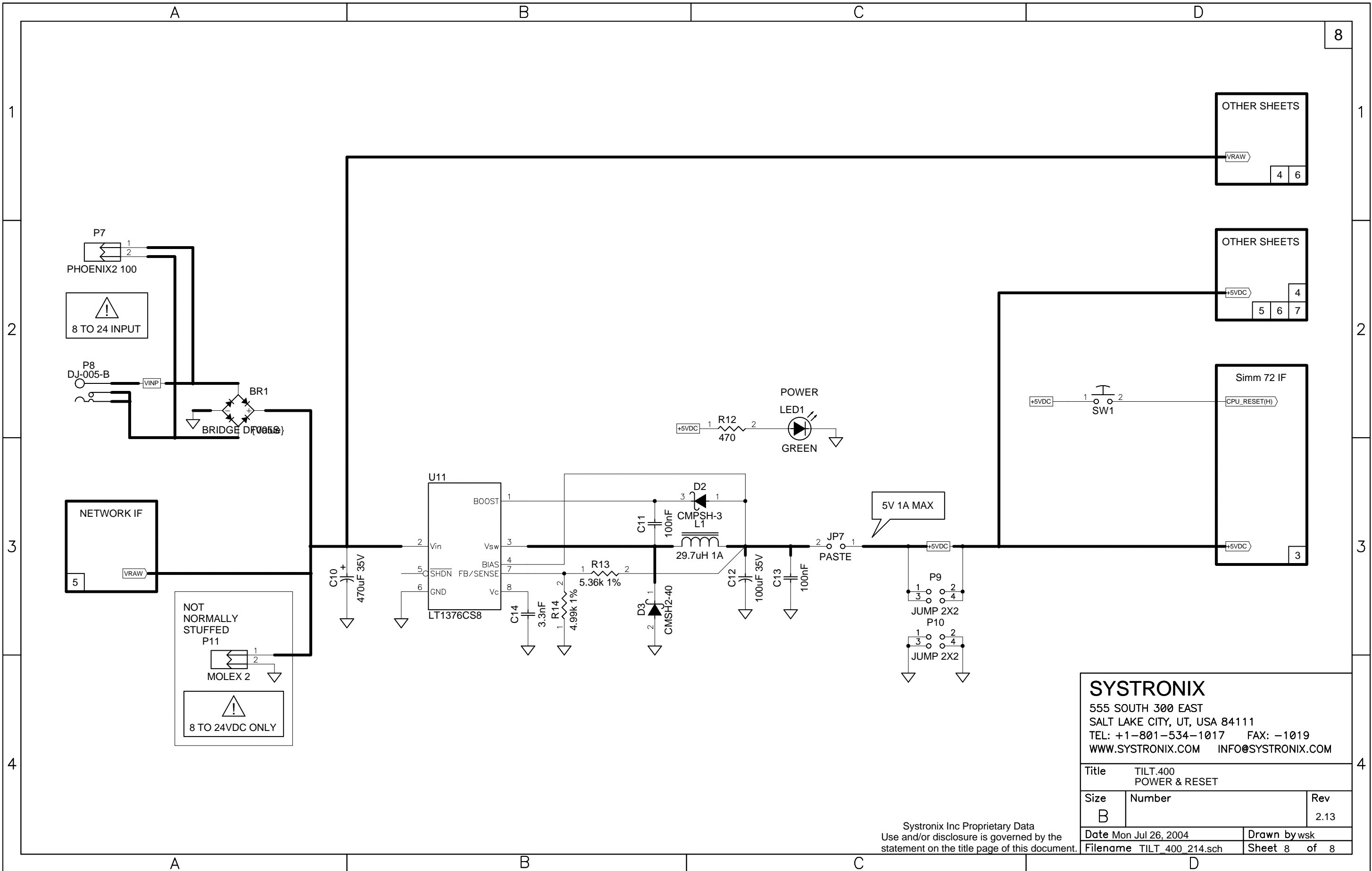


NOTE 4

OPEN ENABLES SERIAL 4 RS-232 XCVR
NOTE 4

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Title TILT.400 SERIAL I/O		
Size B	Number	Rev 2.13
Date Mon Jul 26, 2004	Drawn by bab/wsk	
Filename TILT_400_214.sch	Sheet 7 of 8	



OTHER SHEETS

VRAW	4	6
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OTHER SHEETS

+5VDC	4	
5	6	7

Simm 72 IF

+5VDC	3
CPU_RESET(H)	

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Filename	TILT_400_214.sch	Sheet 8 of 8

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